Embedded Transmission-Line (ETL) MMIC for Low-Cost High-Density Wireless Communication Applications

Hua-Quen Tserng, *Fellow, IEEE*, Paul Saunier, *Senior Member, IEEE*, Andrew Ketterson, *Member, IEEE*, Larry C. Witkowski, *Member, IEEE*, and Ted Jones, *Member, IEEE*

***Abstract*— A new embedded transmission-line (ETL) monolithic-microwave integrated-circuit (MMIC) approach which allows flexibility in mixing different transmission-line types (i.e., coplanar and striplines) for maximum MMIC design flexibility and permits the feasibility of eliminating backside processing for low production cost is described. This ETL MMIC approach is an enabling technology allowing for low-cost batch fabrication, and high-density integration of microwave and RF components (including silicon mixed-signal products) for emerging wireless communication applications. Designs and performance results of a number of ETL MMIC's are described in this paper.**

***Index Terms*— MMIC amplifiers, MMIC phase shifters, MMIC's.**

I. Introduction

ADVANCED microwave multichip assemblies combine monolithic-microwave integrated-circuit (MMIC) chips and other RF components using low-cost batch fabrication and assembly processes. To lower the cost with higher yield, new design concepts other than conventional microstrip-based GaAs MMIC's with chip-and-wire assembly techniques must be used. Greater demand in module packing density requires multichip integration in the vertical dimension, necessitating the use of vertically integratable MMIC components. This is especially true for hand-held communication equipment and phased-array antennas for mobile satellite communications. To lower the thermal impedance of power transistors, flip-chip technique with discrete transistors and backside input/output (I/O) RF pads were reported [1]–[6]. We have conceived and demonstrated an embedded transmission line (ETL) MMIC approach which allows flexibility in mixing different transmission-line types (i.e., coplanar and striplines) for maximum MMIC design flexibility and, in one configuration, permits the elimination of backside processing for low production cost. The ETL MMIC concept, circuit designs, microwave performance, and system applications are described in this paper.

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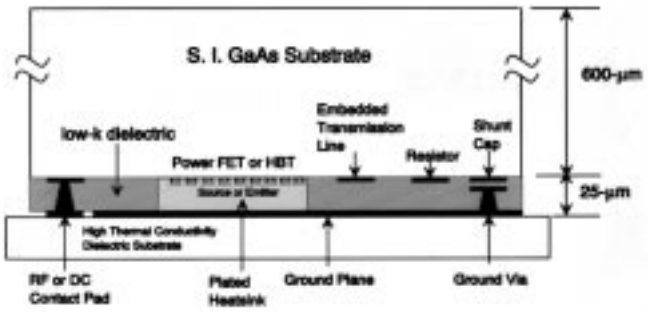


Fig. 1. ETL power MMIC with flipped transistor.

II. ETL MMIC Technology

High-density three-dimensional (3-D) MMIC's with very narrow transmission-line widths and thin polyimide transmission medium were reported [7]. These thin transmission lines generally would incur high insertion losses and are not suitable for high-performance MMIC's. The new ETL MMIC approach utilizes matching circuits with transmission lines and lumped passive components (resistors, series/shunt capacitors, and spiral inductors) embedded in a low-K dielectric (such as polyimide) medium. Fig. 1 shows an ETL MMIC cross section with an unthinned GaAs substrate ($\sim$600 μm). The new MMIC can be used either upright (with the GaAs substrate down) or in inverted configuration (flipped) for flexibility of vertical integration in modules. This approach differs from traditional MMIC design in that transistor sources (FET) or bipolar junction transistor (BJT) emitters are individually grounded to the topside ground plane (through plated heatsink over source or emitter interconnect bridges) to provide excellent heat transfer (in inverted configuration) and low-inductance ground connections. Other passive components such as transmission lines, resistors, and capacitors are fabricated on the GaAs as before—they are redesigned, taking into account the new circuit configuration. Shunt components such as metal–insulator–metal (MIM) capacitors are readily grounded through gold plugs in the thin dielectric rather than the GaAs substrate, as in the conventional MMIC approach. The thickness of the dielectric layer can be on the same order as the plated source/emitter (25–50 μm). For RF I/O and dc biases, connecting pads are isolated from the topside ground plane, allowing for on-wafer testing and flexible interconnections to other module components. No through-GaAs substrate vias (as in the conventional MMIC case) are required for the shunt

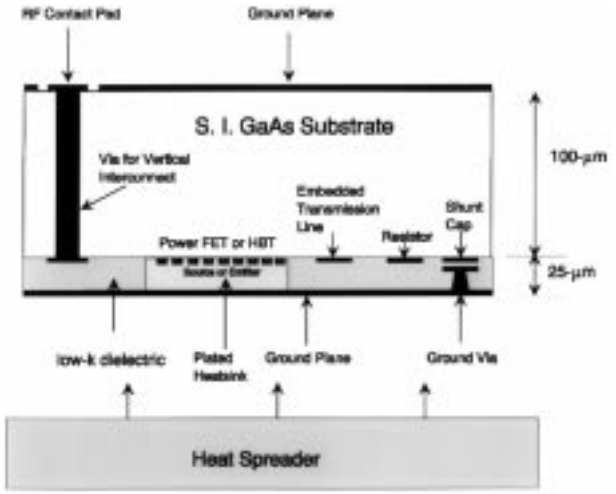


Fig. 2. ETL MMIC with I/O taken from GaAs side.

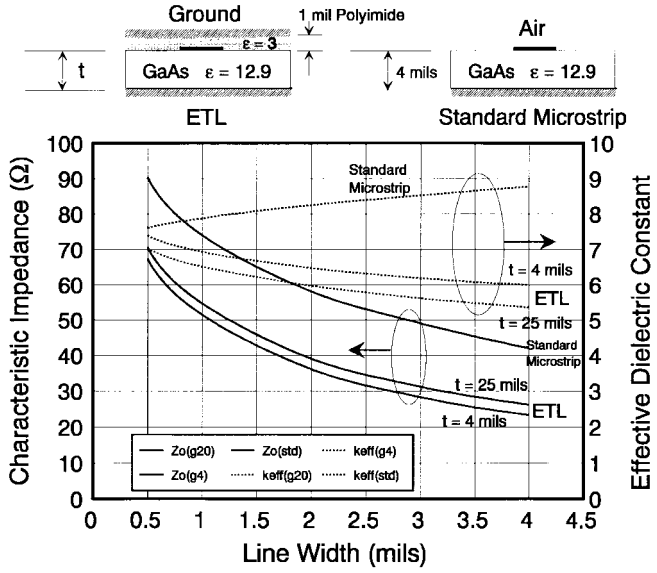


Fig. 3. Transmission-line characteristics.

components, which greatly simplify the process and reduce the costs. If desired, the substrate can be thinned (Fig. 2, showing I/O's through GaAs substrate) and extra ground plane provided to allow desirable I/O pads for vertical integration with other ETL MMIC chips or multilayer distribution board. Thus, the I/O and bias pads can be provided either through the GaAs layer or the polyimide layer, depending on applications.

The characteristics of ETL's were obtained using 3-D electromagnetic simulator software. Fig. 3 shows the characteristic impedance and effective dielectric constant of standard microstrip lines (with 4-mil-thick GaAs substrate) and ETL's with a 1-mil-thick polyimide layer (dielectric constant = 3) for two GaAs substrate thicknesses (4 and 25 mil). As expected, the effect of the thin polyimide layer with its associated ground plane is to lower the characteristic impedance and effective dielectric constant for a given conductor width.

III. ETL MMIC Design, Fabrication, and Performance

Using the above-described ETL MMIC concept, we have demonstrated power amplifiers at 44 GHz, low-noise amplifiers at 20, 28, and 38 GHz, and 4-b phase shifters at 20 and 44 GHz. The 20- and 44-GHz components will be integrated in 20-GHz receive module and 44-GHz transmit module for EHF airborne phased-array antenna applications.

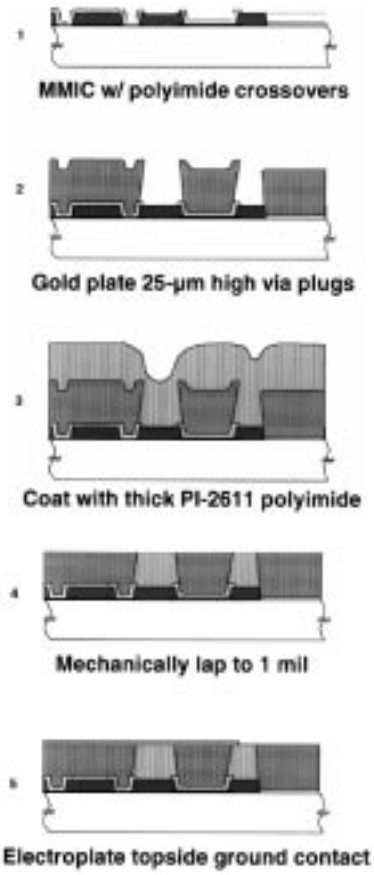


Fig. 4. ETL MMIC processing steps.

A. ETL MMIC Process

The processing steps for the ETL MMIC is shown in Fig. 4. A conventional MMIC processing technique is used up to the source interconnect metal level. Step one shows a polyimide bridge $\sim$6 μm high under the source interconnect. Alternatively, air bridge as in the conventional MMIC can be used. If a polyimide bridge is used, the gap is increased to $\sim$6 μm (instead of $\sim$3 μm for conventional air-bridged MMIC) to minimize the additional parasitic capacitance contributed by the thin polyimide layer. Step two shows the formation of 25-μm-high gold-plated via plugs (for source/emitter interconnect, shunt components ground, RF I/O's, and bias pads). For low-power MMIC's, such as low-noise amplifiers and phase shifters, no thick gold plating for the sources or emitters is necessary for the transistors, as the power dissipation is minimal. To reduce the transmission-line losses (with a wider line), the thick polyimide layer may be increased ($\sim$50 μm) with corresponding thicker plated air bridges (required only for power devices) for the common electrodes. In step three, a thick polyimide (circuit medium) is spun and cured, followed by mechanical lapping to the desired thickness to achieve planarization and dielectric thickness control. The topside

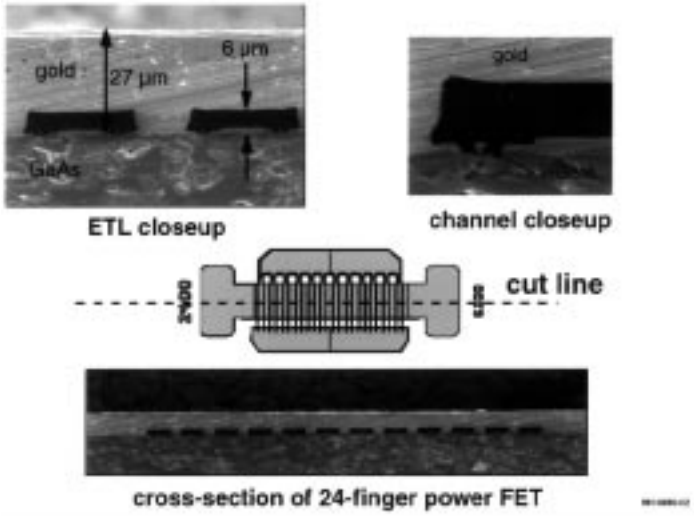


Fig. 5. ETL pHEMT cross section.

ground is then electroplated with via openings for I/O and dc biases. If the ETL MMIC configuration shown in Fig. 2 is desired, the wafer is thinned after completing the above ETL processing steps. Vias are then opened and metallized to access the I/O's and bias pads to the underlying ETL layer. In this way, the active side has a solid ground, a heat sink can readily be attached as in a conventional MMIC, as shown in Fig. 2. In either case, coplanar pads suitable for on-wafer RF characterization are provided on either the GaAs or polyimide ground-plane side. Fig. 5 shows cross-sectional SEM photographs of a 0.25 μm $\times$ 2400 μm (24 gate fingers) power pseudomorphic high electron-mobility transistor (pHEMT) with polyimide bridges and $\sim$29-μm-thick plated source bridges. The integrity of the ETL process is clearly seen. In the case of low-power MMIC's, in liu of the thick plated gold, thinner interconnected bridges (since no heat sink is required), as in a conventional MMIC with overlaying polyimide, is used to simplify the processing steps.

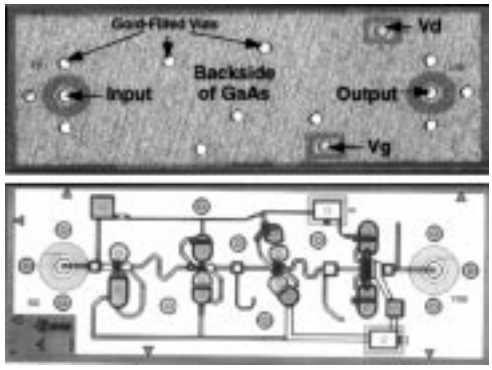
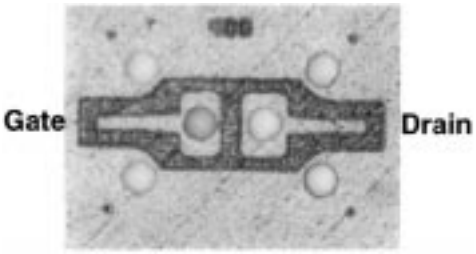
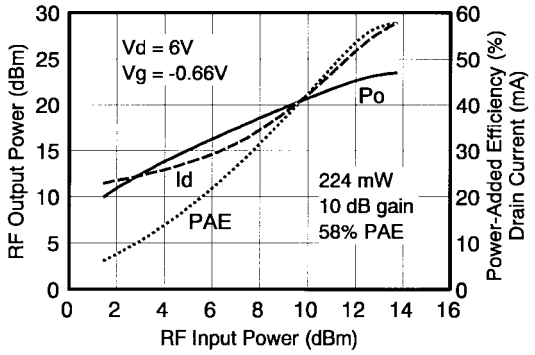


Fig. 6. 44-GHz four-stage ETL MMIC amplifier. Gatewidths: 50, 100, 200, and 400 μm.



(a)



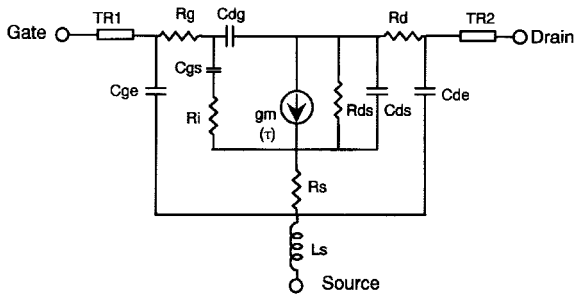
(b)

Fig. 7. 400-μm ETL pHEMT. (a) Configuration. (b) Performance.

B. ETL MMIC Designs and Performance

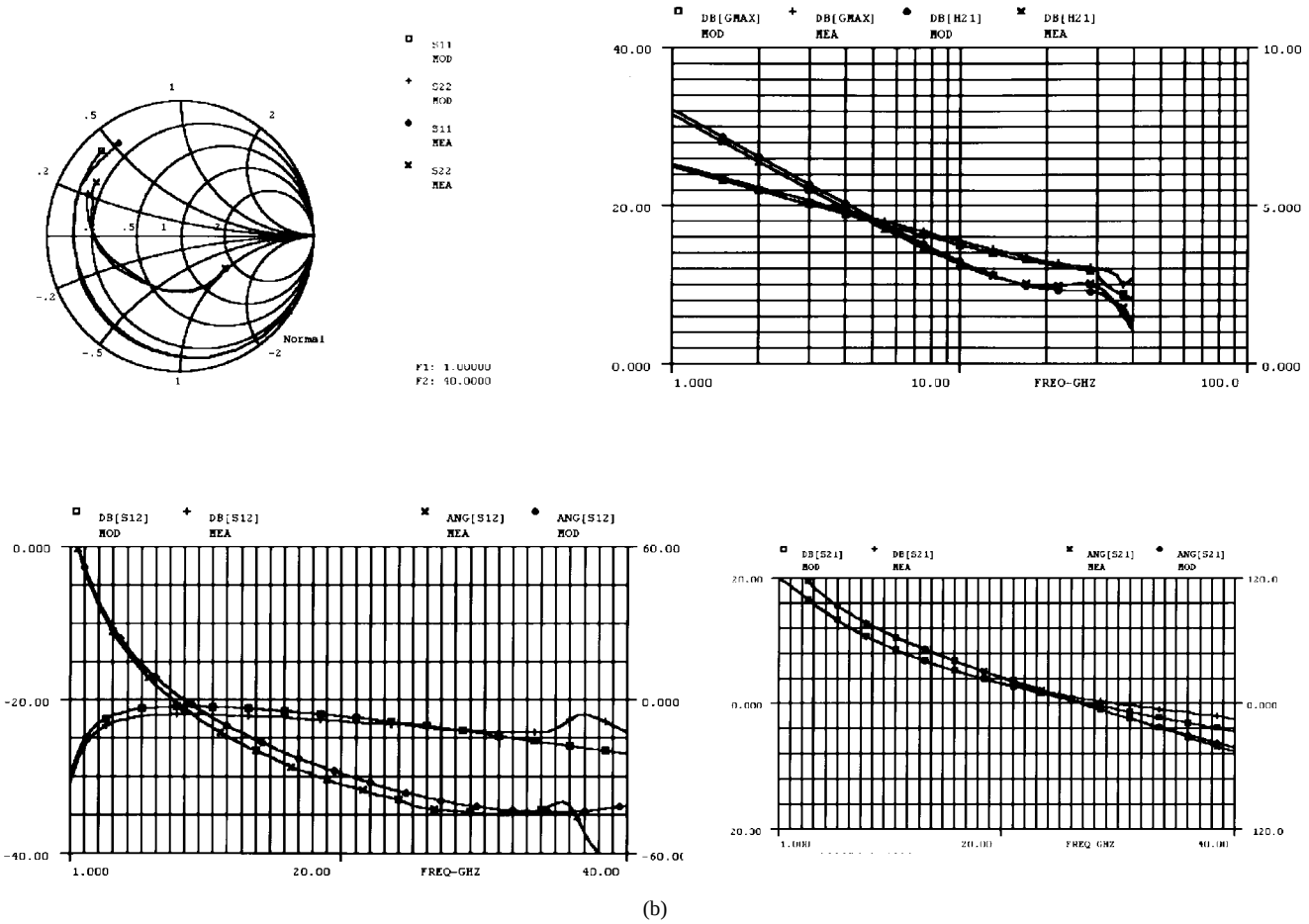
AlGaAs/InGaAs on GaAs (pHEMT) technology was used for demonstrating our ETL MMIC approach. Other device technology such as HBT can also be used to take advantage of the new MMIC configuration. As in conventional MMIC's, the pHEMT's are used for power, low-noise amplifications, and switches (for phase shifters). The device topology and channel processing parameters have been optimized for their respective MMIC applications. The circuit-design technique is similar to that of conventional MMIC's by using S-parameters, large-signal load-pull and noise parameter data, and switching characteristics (on resistance and off capacitance). All of the MMIC designs to be described next are based on 25-μm-thick polyimide and 4-mil-thick (100 μm) GaAs substrate. The intended applications for these MMIC's dictate that planar RF I/O's and bias pads be provided with adjacent ground planes to allow for vertical integration/connection with other RF/dc or logic distribution boards or MMIC's. Discrete ETL devices were on-wafer characterized for MMIC designs. The impedance and effective dielectric constant plots shown in Fig. 3 provide the needed information for ETL MMIC designs.

1) Power Amplifiers: Fig. 6 shows an ETL Q-band four-stage MMIC amplifier using 50 μm/100 μm/200 μm/400 μm gatewidth pHEMT's. The gate length is 0.25 μm. The lower picture shows the front or active side (with the 1-mil-thick polyimide removed) of the MMIC chip. The top picture shows the backside of the GaAs with RF I/O pads and bias pads. The GaAs substrate thickness is 4 mil. The chip size is 60 mil $\times$ 160 mil. The MMIC was mounted with the polyimide-side ground plane down to the heatsink. Stable amplifier operation was obtained at 44.5 GHz (the design center frequency) with up to 27-dB small-signal gain (1-dB bandwidth = 1.5 GHz). With increased input drive, an output power of 100 mW with 20-dB gain was achieved. This ETL MMIC will be vertically integrated with the ETL phase-shifter MMIC on the backside (stacked) for Q-band transmitter array applications. Discrete 400 μm ETL pHEMT device from the same wafer was flip-chip mounted and tested at 20 GHz.



Rg	Ri	Cgs	Cdg	gm	Tau	Rs	Rds	Cds	Rd	Ls	Cge	Cde
0.2	0.4	0.71	0.06	257	1.88	2.6	70	0.04	3.5	.006	0.00	0.17

(a)



(b)

Fig. 8. Modeled and measured S-parameters of a 400-μm ETL pHEMT. (a) Device model. (b) Modeled and measured S-parameters. $V_d = 3$ V, $I_d = 60$ mA, $V_g = -0.35$ V.

Fig. 7(a) shows the I/O's on the backside (GaAs). Fig. 7(b) shows the microwave performance. The device achieved an output power of 224 mW with 10-dB gain and 58% power-added efficiency at 20 GHz. Fig. 8(a) and (b) shows the measured and modeled S-parameters of an ETL 400 μm gatewidth unit cell. The equivalent-circuit element values deduced from the S-parameters are also shown.

2) Low-Noise Amplifiers: ETL low-noise amplifiers at K-, Ka-, and Q-band were also demonstrated. Fig. 9 shows a K-band three-stage ETL MMIC low-noise amplifier with 150-μm gatewidth pHEMT in each stage. The ETL MMIC chip (60 mil $\times$ 162 mil) achieved a gain of $\sim$30 dB (biased for gain) over the 19–28-GHz frequency band (Fig. 10). Fig. 11 shows the noise performance. A noise figure of 1.2 dB with 25-dB gain was obtained at 22 GHz. The noise figure remains below 2 dB up to 25 GHz. A four-stage amplifier (from another wafer) with the same chip size (Fig. 12) achieved a gain of $\sim$33 dB with 1.4-dB noise figure at 22 GHz. Fig. 13 shows the typical gain and noise performance across the 18–26-GHz band. Over the design bandwidth of 20–22 GHz, the average noise figure

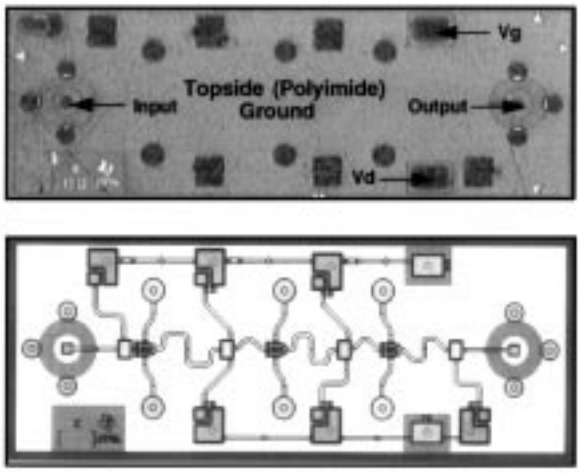


Fig. 9. A three-stage K-band ETL MMIC low-noise amplifier.

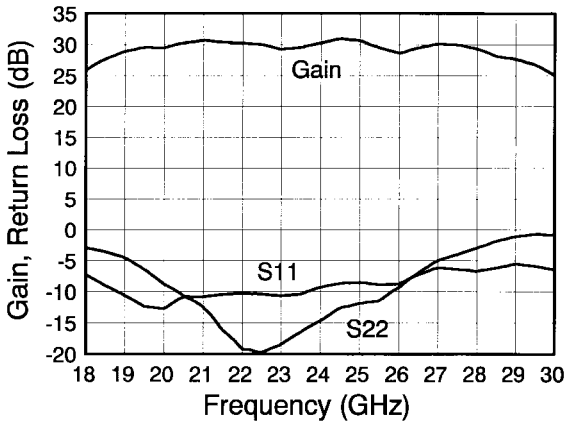


Fig. 10. Gain-frequency response of a K-band three-stage pHEMT ETL MMIC amplifier.

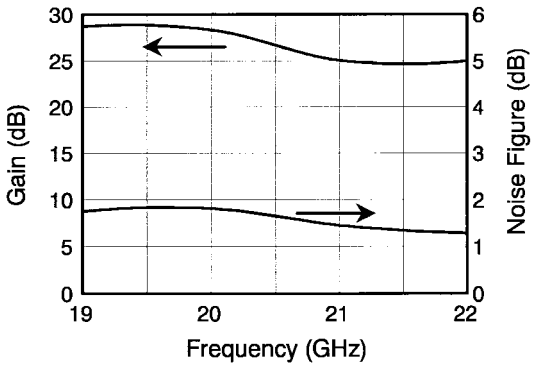


Fig. 11. Noise performance of a K-band three-stage pHEMT ETL MMIC amplifier ($V_d = 2$ V, $I_d = 37$ mA).

is ~1.5 dB. The noise figure remains below 2 dB over most of the 18–26-GHz frequency band. Other amplifiers using 100-μm device in each stage on the same mask achieved gains of up to 25–30 dB over a very broad band centered at 28 and 36 GHz. Fig. 14 shows the gain performance of a Ka-band three-stage design when biased for gain. As shown, a gain of ~30 dB over a very broad band is obtained. The noise performance of this amplifier was not measured. In these amplifier design, series feedback with source inductance was used in each stage for stability. In addition, for the first

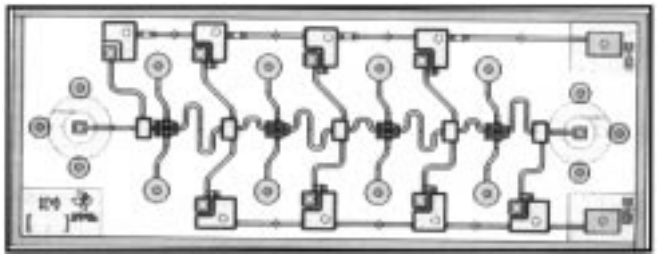


Fig. 12. Four-stage K-band ETL MMIC low-noise amplifier.

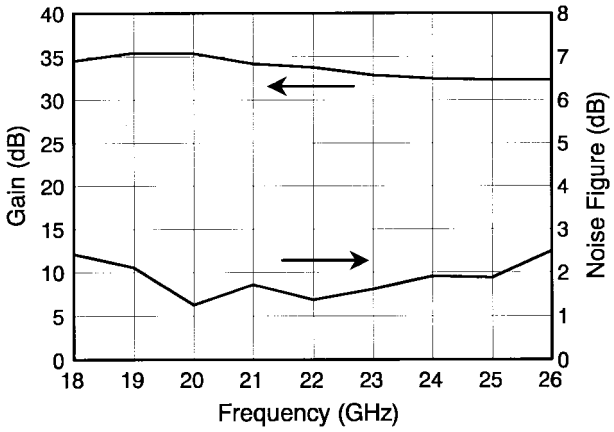


Fig. 13. Performance of four-stage ETL MMIC low-noise amplifier.

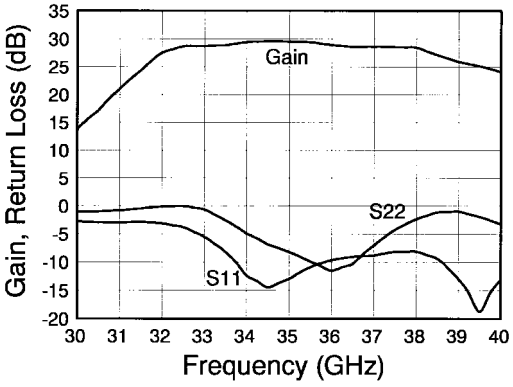


Fig. 14. Performance of Ka-band three-stage ETL MMIC amplifier.

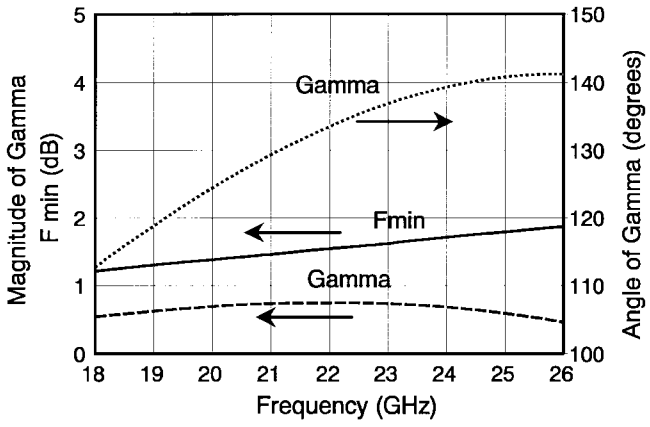


Fig. 15. $F_{\min}$ and Γ_{opt} of a 150-μm pHEMT. $V_d = 3$ V, $I_d = 9.9$ mA.

stage, this feedback inductance also provides simultaneous noise and conjugate match for the first stage. On-wafer noise

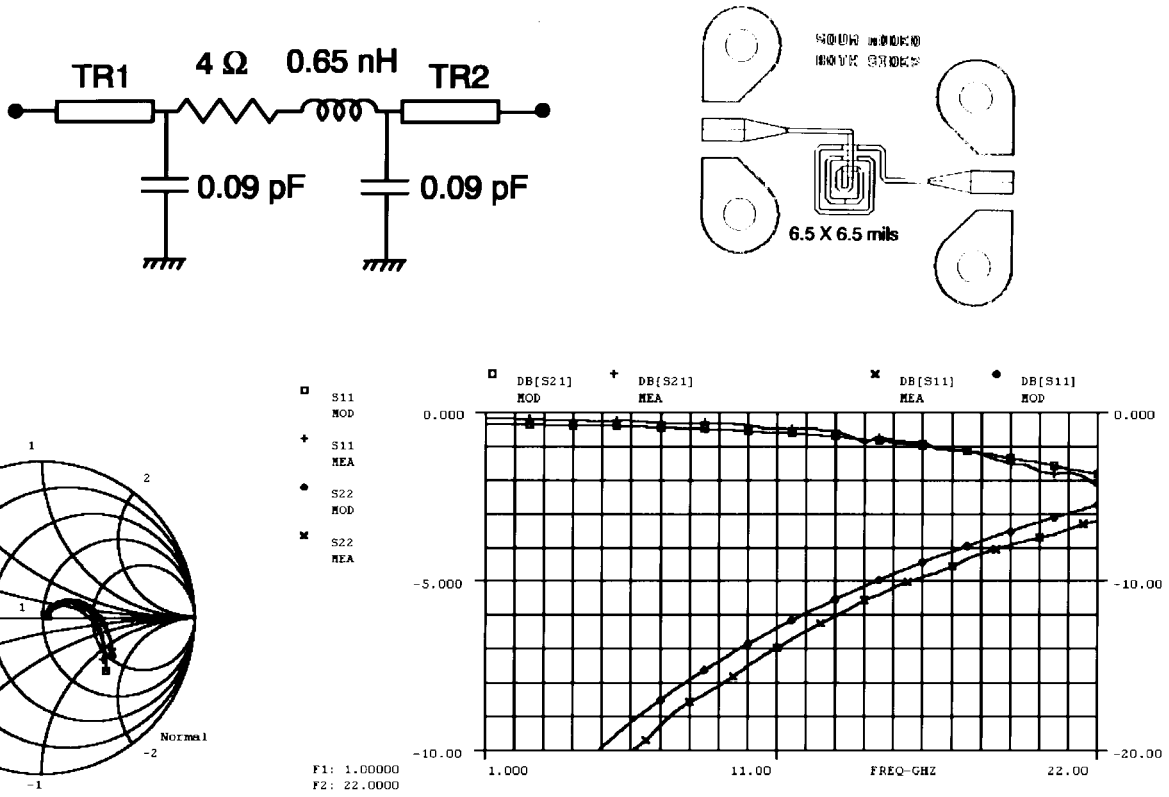


Fig. 16. ETL spiral inductor.

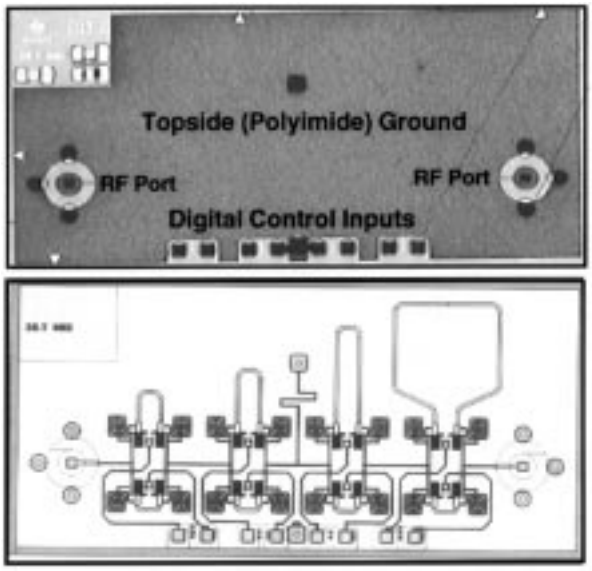


Fig. 17. K-band 4-b ETL MMIC phase shifter. Size: 86 mil × 176 mil.

characterization was used for both discrete devices and MMIC amplifiers. Fig. 15 shows the $F_{\min}$ and Γ_{opt} plot of a 150-μm ETL device. Depending on the bias conditions, the $F_{\min}$ can be as low as 1 dB at 22 GHz. With circuit loss taken into account, our achievement of a noise figure of 1.2–1.5 dB is considered to be excellent.

3) Phase Shifters: In addition to power and low-noise amplifiers, we also demonstrated ETL MMIC phase shifters at K- and Q-band frequencies. pHEMT switches with source and drain at ground potential were used in a switched-line phase-shifter configuration. An eight-finger (44-μm unit gate finger width), 352-μm gatewidth pHEMT was used as the switch. An on-resistance of ∼7 Ω and an off-capacitance of ∼0.08 pF were obtained by S-parameter measurements and modeling. To improve the isolation, when the device is pinched off, an inductor in parallel with the device was used. For K-band operation, the inductance was realized with a three-turn spiral shown in Fig. 16. Both the line width and gapwidth are 0.5 mil. The ETL spiral inductor (with 1-mil-thick polyimide overlay and 4-mil-thick GaAs substrate) was characterized and modeled. Fig. 16 shows the two-terminal inductor layout and equivalent circuit parameters. Modeled and measured 2-port S-parameters are also shown. While the series resistance of 4 Ω is similar to that of a conventional MMIC without polyimide overlay, the inductance is decreased from 0.8 to 0.65 nH. The shunt capacitance is also increased by ∼50%. This equivalent circuit model was used to design a 4-b phase shifter at K-band. Each bit uses two single-pole double-throw (SPDT) switches to ensure adequate isolation between the on and off paths. Fig. 17 shows a chip layout and photograph of the topside (polyimide) configuration of the K-band phase shifter. As shown, switched lines with pHEMT switches are used. Since the pHEMT is operated at zero bias, no dc power is consumed. The chip measures 86 mil × 176 mil, including RF transitions for vertical integration with other multilevel circuit board. Fig. 18 shows the performance (insertion phase, return losses, and insertion loss) of the four major phase states. Excellent insertion phase performance is achieved at the design-center frequency of 21 GHz. With an improved I/O matches the insertion loss is expected to be much less than 10 dB. Our

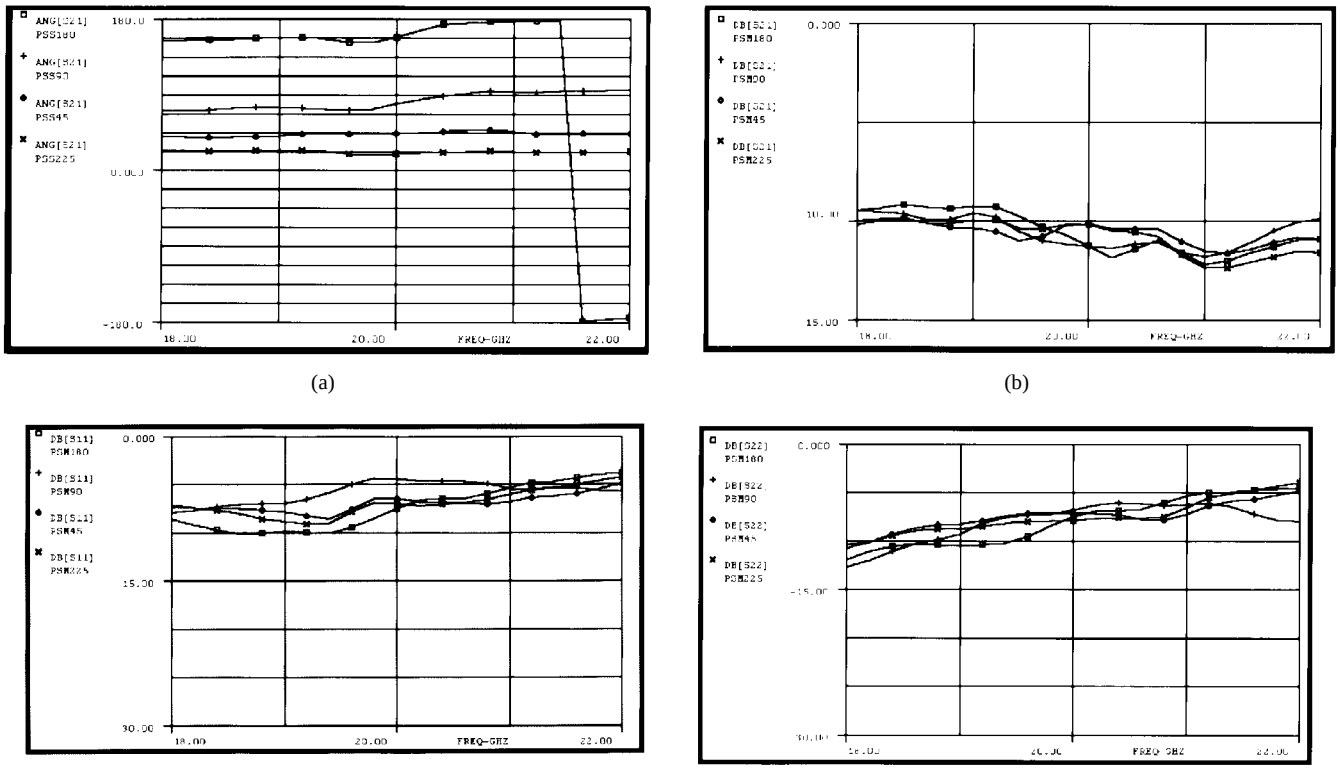


Fig. 18. Performance of K-band 4-b ETL MMIC phase shifter. (a) Insertion phase (degrees). (b) Insertion loss (dB). (c) Port one return loss (dB). (d) Port two return loss (dB).

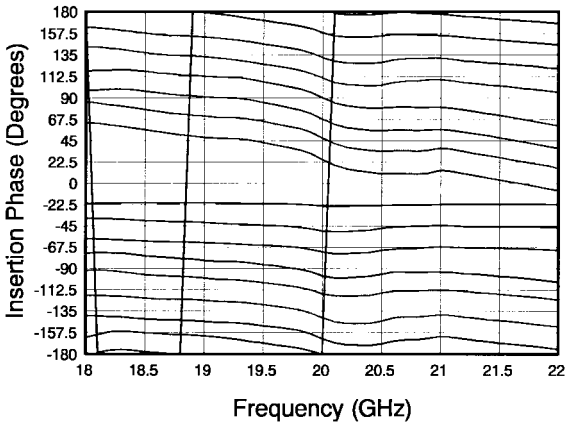


Fig. 19. Phase performance of K-band 4-b ETL MMIC phase shifter.

latest design with I/O matching stubs has shown more than 20-dB return loss in the design frequency band. Fig. 19 shows the performance of all phase states. The circuit layout of the Q-band 4-b phase shifter is shown in Fig. 20. The chip measures 61 mil $\times$ 138 mil. The resonant frequency for the off-arm is achieved by a high-impedance transmission-line loop. Fig. 21 shows the performance of the 1-b phase shifters included on the same mask as the 4-b phase shifter. The phase and VSWR performance are excellent for the first-pass design. The insertion loss can be reduced by further minimizing the on-resistance of the pHEMT. The performance of the Q-band 4-b phase shifter is shown in Fig. 22. Deviations of the 45° and 90° bits are caused by proximity coupling from a dc return pass as the measured individual phase bits are very close to

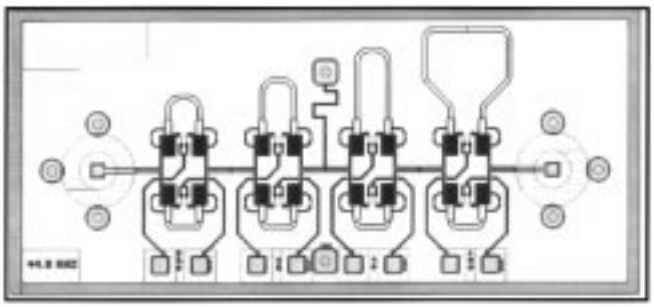


Fig. 20. Q-band 4-b ETL MMIC phase shifter.

the design value (shown in Fig. 21). Rerouting of the dc return pass is expected to improve the phase responses.

IV. System Applications of ETL MMICs

The ETL MMIC's described above have been developed to demonstrate low-cost ultra-compact solid-state transmit and receive phased-array modules for advanced airborne phased-array communication applications. Since only coplanar I/O's and bias pads are used for the ETL MMIC, it is very suitable for low-cost batch fabrication, and integration with multilayer board (for RF and dc distribution and control signals) by using surface mounting technique for chip-to-board or chip-to-chip (stacked MMIC) interconnection without using bonding wires. For single-function applications, we also demonstrated the performance of low-noise and power ETL MMIC amplifiers with 25-mil-thick unthinned GaAs substrate. Multiwatt X-band MMIC's were also demonstrated. The results will be

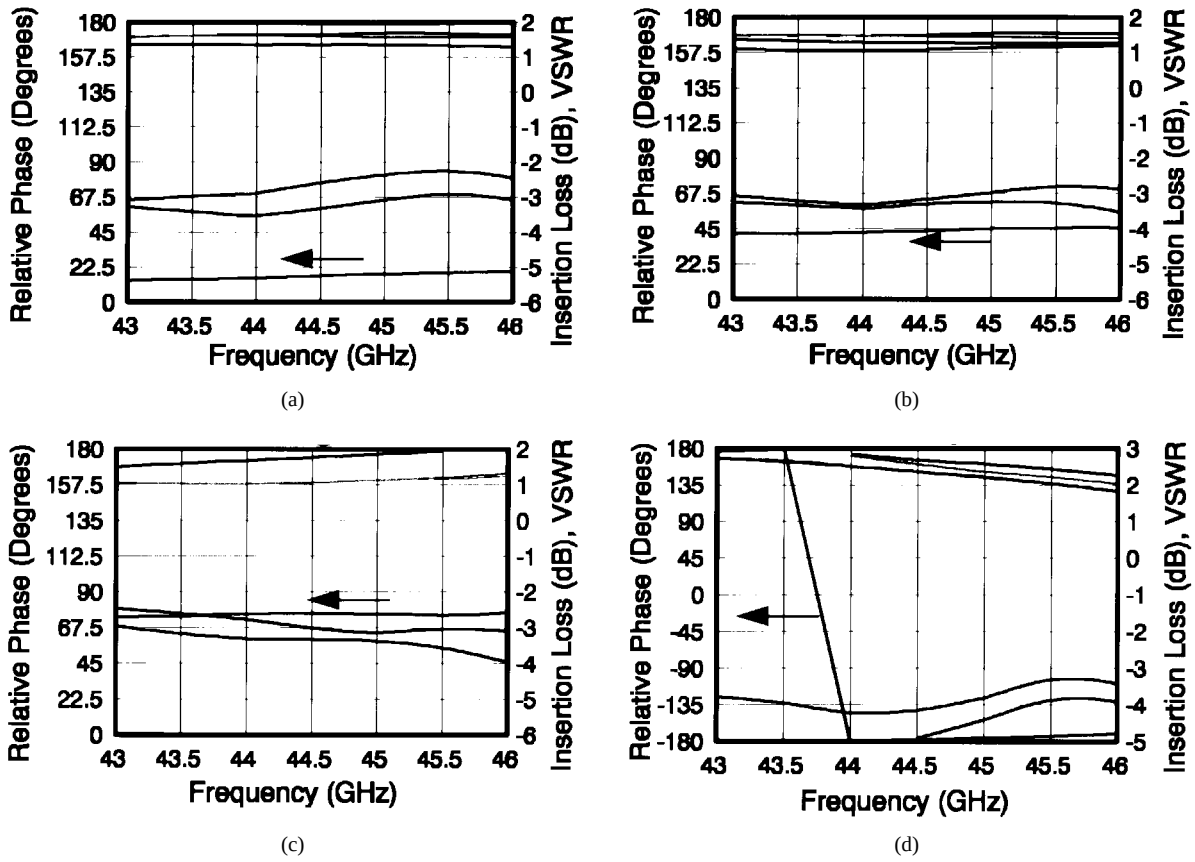


Fig. 21. Q-band 1-b ETL MMIC phase shifters. (a) 22.5°. (b) 45°. (c) 90°. (d) 180°.

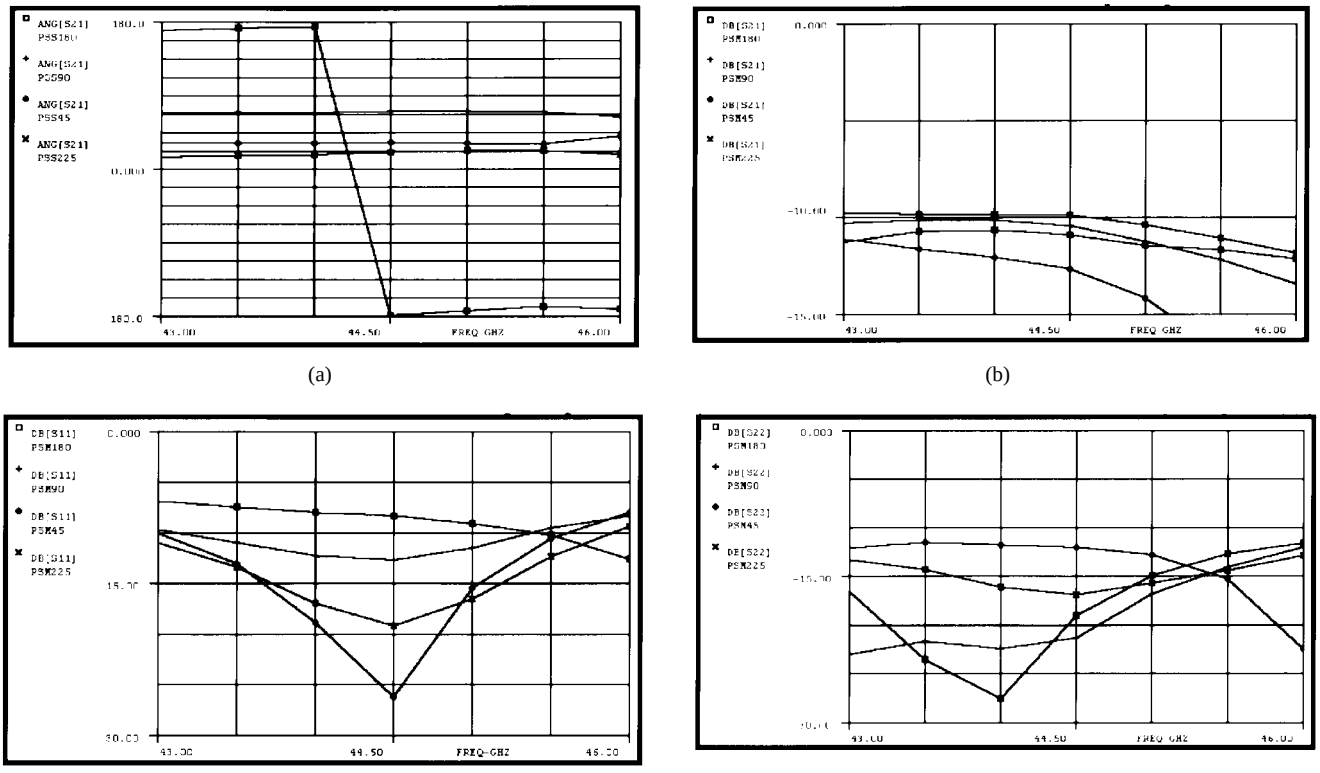


Fig. 22. Performance of Q-band 4-b ETL MMIC phase shifter. (a) Insertion phase (degrees). (b) Insertion loss (dB). (c) Port one return loss (dB). (d) Port two return loss (dB).

described in future publications. Thus, we have shown that it is feasible to design a MMIC without backside processing (wafer thinning, via etch, and plating), resulting in significant cost savings in production.

V. Conclusions

Our newly developed ETL MMIC approach is an enabling technology allowing for low-cost batch fabrication, and high-density integration of microwave/millimeter-wave and RF components (including silicon mixed-signal products) for military radar, electron warfare (EW), and emerging commercial wireless communication applications. The same concept can also be used for high-speed clock distributions of silicon IC's. Because of the quasi-hermetic nature of the ETL MMIC, it also simplifies the packaging requirement with resulting lower cost. Application areas include: wireless cable systems [such as 28-GHz local multipoint distribution service (LMDS)], wireless local-area network (WLAN), mobile satellite communications, and automotive radar @77 GHz.

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